2. Pin Functions

This section discusses the TMS34010 pin functions. Section 2.1 contains a TMS34010 pinout, summarizes the pin functions, and associates the pins with various categories. Section 2.2 through Section 2.6 present details concerning the individual categories. Contents of this section include:

Section **Page**

2.1 Pinout and Pin Descriptions

The TMS34010 is packaged as a 68-pin plastic leaded chip carrier (PLCC). Figure 2-1 shows a pinout of the TMS34010 processor. Mechanical information is contained in Appendix A.

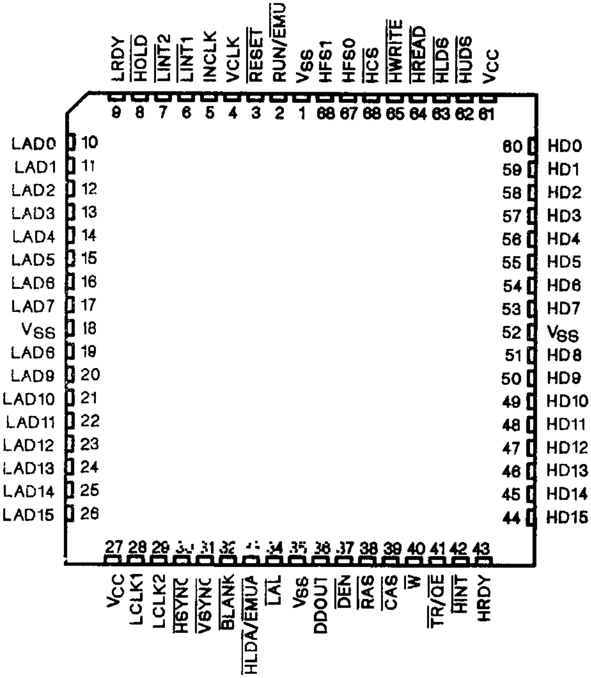


Figure 2-1. TMS34010 Pinout (Top View)

The TMS34010's 68 pins are divided among several interfaces:

Host interface	25 pins
Local memory interface	29 pins
Video timing interface	4 pins
Hold and emulator interfaces	3 pins
Power and reset	7 pins
Total:	68 pins

Figure 2-2 associates the pins with the TMS34010's major interfaces. Table 2-1 summarizes the pin functions at each interface.

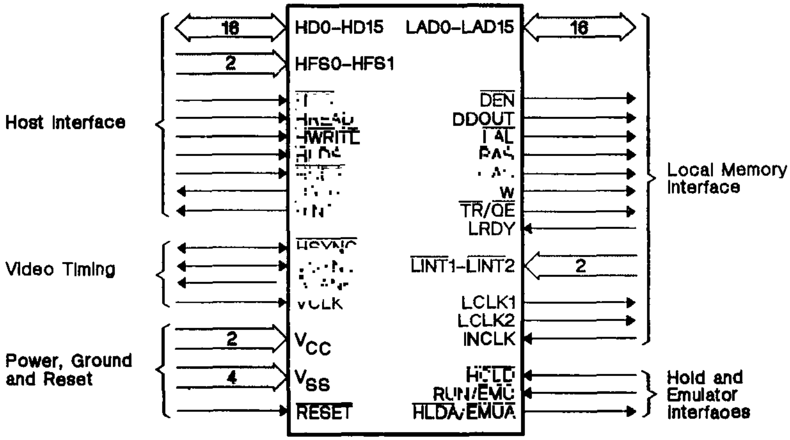


Figure 2-2. TMS34010 Major Interfaces

Table 2-1. Pin Descriptions

Name	Pin	I/O	Description
Host Interface Bus Pins			
$\overline{\text{HCS}}$	66	I	Host chip select
HD0–HD15	44–51,53–60	I/O	Host bidirectional data bus
HFS0,HFS1	67,68	I	Host function select
$\overline{\text{HINT}}$	42	O	Host interrupt request
$\overline{\text{HLDS}}$	63	I	Host lower data select
$\overline{\text{HUDS}}$	62	I	Host upper data select
HRDY	43	O	Host ready
$\overline{\text{HREAD}}$	64	I	Host read strobe
$\overline{\text{HWRITE}}$	65	I	Host write strobe
Local Interface Bus Pins			
$\overline{\text{RAS}}$	38	O	Local row-address strobe
$\overline{\text{CAS}}$	39	O	Local column-address strobe
DDOUT	36	O	Local data direction out
$\overline{\text{DEN}}$	37	O	Local data enable
LAD0–LAD15	10–17,19–26	I/O	Local address/data bus
$\overline{\text{LAL}}$	34	O	Local address latched
LCLK1,LCLK2	28,29	O	Local output clocks
$\overline{\text{LINT1}}$,$\overline{\text{LINT2}}$	6,7	I	Local interrupt request pins
LRDY	9	I	Local ready
$\overline{\text{TR}}$/$\overline{\text{QE}}$	41	O	Local shift-register transfer or output enable
$\overline{\text{W}}$	40	O	Local write strobe
INCLK	5	I	Input clock
Hold and Emulation			
$\overline{\text{HOLD}}$	8	I	Hold request
RUN,$\overline{\text{EMU}}$	2	I	Run/Emulate
$\overline{\text{HLDA}}$,$\overline{\text{EMUA}}$	33	O	Hold acknowledge or emulate acknowledge
Video Timing Signals			
$\overline{\text{BLANK}}$	32	O	Blanking
$\overline{\text{HSYNC}}$	30	I/O	Horizontal sync
VCLK	4	I	Video clock
$\overline{\text{VSYNC}}$	31	I/O	Vertical sync
Miscellaneous			
$\overline{\text{RESET}}$	3	I	Device reset
V_{CC}	27,61	I	Nominal 5-volt power supply
V_{SS}	1,18,35,52	I	Ground

2.2 Host Interface Bus Signals

The host interface pins are used for communication between the TMS34010 and a host processor. Signals output on these pins are assumed to be asynchronous with respect to local clocks LCLK1 and LCLK2. To software running on a host processor, the TMS34010's host interface appears as a peripheral device containing a block of four 16-bit registers. Table 2-2 describes the host interface pins. TMS34010 host interface operation is discussed in Section 10. Host interface registers are discussed in Section 6.

Table 2-2. Host Interface Signals

Signal	I/O	Description
$\overline{\text{HCS}}$	I	*Host Chip Select.* $\overline{\text{HCS}}$ is driven active low to enable access to the 16-bit host interface register that is selected by HFS0 and HFS1. During the low-to-high transition of $\overline{\text{RESET}}$, the level on the $\overline{\text{HCS}}$ input determines whether the TMS34010 is halted (if $\overline{\text{HCS}}$ is high), or begins immediately executing its reset service routine (if $\overline{\text{HCS}}$ is low).
HFS0–HFS1	I	*Host Function Select.* The two function select pins determine which of the four 16-bit host interface registers is selected during a read or write cycle that is initiated by the host processor. **HFS1 HFS0 Register Description** 0 0 HSTADRL LSBs of pointer address 0 1 HSTADRH MSBs of pointer address 1 0 HSTDATA Data buffer register 1 1 HSTCTL Control register
$\overline{\text{HREAD}}$	I	*Host Read Strobe.* $\overline{\text{HREAD}}$ is driven active low during a read cycle that is initiated by the host processor. This enables the contents of the selected host interface register to be output on HD0–HD15. $\overline{\text{HREAD}}$ should not be active low at the same time that $\overline{\text{HWRITE}}$ is active low.
$\overline{\text{HWRITE}}$	I	*Host Write Strobe.* $\overline{\text{HWRITE}}$ is driven active low during a write cycle that is initiated by the host processor. This enables the contents of HD0–HD15 to be written to the selected host interface register. $\overline{\text{HWRITE}}$ should not be active low at the same time that $\overline{\text{HREAD}}$ is active low.
$\overline{\text{HLDS}}$	I	*Host Lower Data Select.* $\overline{\text{HLDS}}$ is driven active low during a read or write cycle that is initiated by the host. This enables the lower byte (bits 0–7) of the selected host interface register to be accessed.
$\overline{\text{HUDS}}$	I	*Host Upper Data Select.* $\overline{\text{HUDS}}$ is driven active low during a read or write cycle that is initiated by the host processor. This enables the upper byte (bits 8–15) of the selected host interface register to be accessed.
HRDY	O	*Host Ready.* HRDY indicates when the TMS34010 is ready to complete a read or write cycle that is initiated by the host. Except during an access of a host interface register, HRDY is always high. HRDY will be driven low if the host processor attempts to initiate an access of a host interface register before the TMS34010 has had sufficient time to complete all processing resulting from an access initiated previously by the host. HRDY always goes low briefly at the start of a HSTCTL register access. When HRDY is driven low, the host must wait to complete the access until HRDY is again driven high. While $\overline{\text{HCS}}$ is high, HRDY is driven high.

Table 2-2. Host Interface Signals (Concluded)

Signal	I/O	Description
$\overline{\text{HINT}}$	O	*Host Interrupt Request.* The $\overline{\text{HINT}}$ pin follows the INTOUT bit in the HSTCTL register. $\overline{\text{HINT}}$ is typically used to transmit interrupt requests from the TMS34010 to the host processor. When INTOUT is set to 1 by the TMS34010, $\overline{\text{HINT}}$ is driven active low. $\overline{\text{HINT}}$ remains active low until the host writes a 0 to INTOUT, at which time $\overline{\text{HINT}}$ becomes inactive high.
HD0–HD15	I/O	*Host Bidirectional Data Bus.* The host data pins, HD0–HD15, form a bidirectional 16-bit bus. This bus is used to transfer data between the selected 16-bit host interface register and the host processor. HD0 is the LSB and HD15 is the MSB.

2.3 Local Memory Interface Signals

The TMS34010 uses the local bus interface pins to communicate with external memory and with external memory-mapped I/O devices. The signals at this interface are used directly to control DRAMs (dynamic RAMs) and VRAMs (video RAMs). Local memory interface operation is discussed in Section 11.

Table 2-3. Local Bus Interface Signals

Signal	I/O	Description
$\overline{\text{DEN}}$	O	*Local Data Enable.* $\overline{\text{DEN}}$ is an active-low output. It is used to drive the active-low output-enable inputs on the bidirectional transceivers (such as the 74ALS245), which are used to buffer data input and output on the LAD0–LAD15 pins. External buffering may be required on the LAD0–LAD15 pins when the TMS34010 is interfaced to a large number of local memory devices.
DDOUT	O	*Local Data Direction Out.* DDOUT drives the direction control inputs on the bidirectional transceivers (such as the 74ALS245), which are used to buffer data input and output on the LAD0–LAD15 pins. External buffering may be required on the LAD0–LAD15 pins when the TMS34010 is interfaced to a large number of local memory devices. During write cycles, DDOUT is driven high to enable data to be output from the LAD0–LAD15 pins while $\overline{\text{DEN}}$ is driven active low. During read cycles, DDOUT goes low to enable data to be input to the LAD0–LAD15 pins while $\overline{\text{DEN}}$ is driven active low. At all other times, DDOUT remains driven to the default high level.
$\overline{\text{LAL}}$	O	*Local Address Latched.* An external latch can use the high-to-low transition of $\overline{\text{LAL}}$ to capture the column address from the LAD0–LAD15 pins. When a transparent latch such as a 74ALS373 is used, the address remains latched as long as $\overline{\text{LAL}}$ remains active low.
$\overline{\text{RAS}}$	O	*Local Row Address Strobe.* The $\overline{\text{RAS}}$ output is used to drive the $\overline{\text{RAS}}$ inputs of DRAMs and VRAMs.
$\overline{\text{CAS}}$	O	*Local Column Address Strobe.* The $\overline{\text{CAS}}$ output is used to drive the $\overline{\text{CAS}}$ inputs of DRAMs and VRAMs.
$\overline{\text{W}}$	O	*Local Write Strobe.* The active-low $\overline{\text{W}}$ output is used to drive the $\overline{\text{W}}$ inputs of DRAMs and VRAMs. $\overline{\text{W}}$ can also be used as the active-low write enable to static memories and other devices connected to the TMS34010 local interface. During a local memory read cycle, $\overline{\text{W}}$ remains inactive high while $\overline{\text{CAS}}$ is strobed active low. During a local memory write cycle, $\overline{\text{W}}$ is strobed active low while $\overline{\text{CAS}}$ is low. During shift-register-transfer cycles, the state of $\overline{\text{W}}$ indicates whether the transfer is from shift register to memory ($\overline{\text{W}}$ is low) or memory to shift register ($\overline{\text{W}}$ is high). At all other times, $\overline{\text{W}}$ is driven to the default high level.
$\overline{\text{TR}}/\overline{\text{QE}}$	O	*Local Shift Register Transfer or Output Enable.* This pin connects directly to the $\overline{\text{TR}}/\overline{\text{QE}}$ (or $\overline{\text{DT}}/\overline{\text{OE}}$) pin of a VRAM. During local memory read cycles, $\overline{\text{TR}}/\overline{\text{QE}}$ functions as an active-low output enable to gate data from memory to the LAD0–LAD15 pins. During VRAM shift-register-transfer cycles, $\overline{\text{TR}}/\overline{\text{QE}}$ is driven active low during the high-to-low transition of $\overline{\text{RAS}}$.
INCLK	I	*Input Clock.* INCLK is the input clock used to generate the LCLK1 and LCLK2 outputs, to which all processor functions in the TMS34010 are synchronous. A separate input clock, VCLK, controls the video timing registers.

Table 2-3. Local Bus Interface Signals (Concluded)

Signal	I/O	Description
LCLK1,LCLK2	O	*Local Output Clocks.* These two output clocks, 90 degrees out of phase with each other, provide convenient synchronous control of external circuitry to the TMS34010's internal timing. All signals output from the TMS34010, with the exception of the CRT timing signals, are synchronous to these clocks.
LRDY	I	*Local Ready.* LRDY is driven low by external circuitry to inhibit the TMS34010 from completing a local memory cycle it has initiated. While LRDY remains low, the TMS34010 continues to wait. When LRDY is again driven high, the TMS34010 completes the cycle. While LRDY is low, the TMS34010 generates internal wait states in increments of one full LCLK1 cycle in duration. LRDY can be driven low to extend local memory read and write cycles, shift-register-transfer cycles, and DRAM refresh cycles. During internal cycles, the TMS34010 ignores LRDY.
$\overline{\text{LINT1}}$,$\overline{\text{LINT2}}$	I	*Local Interrupt Request Pins.* Interrupt requests from external devices are transmitted to the TMS34010 on the $\overline{\text{LINT1}}$ and $\overline{\text{LINT2}}$ pins. Each pin activates the request for one of two external interrupt request levels. An external device generates an interrupt request by driving the appropriate interrupt request pin to its active-low state. The pin should remain active low until the TMS34010 has recognized the request. Transitions on the two interrupt request pins are assumed to be asynchronous with respect to local clocks LCLK1 and LCLK2; the signals on these pins are synchronized internally before being used internally. The local interrupt pins are reconfigured during emulation and testing to perform special functions that are described in a separate emulation and testing document.
LAD0–LAD15	I/O	*Local Address/Data Bus.* LAD0–LAD15 form the local multiplexed address/-data bus. At the start of a memory cycle, two addresses (row and column) are output on LAD0–LAD15. During a read cycle, data are input on LAD0–LAD15 during the latter part of the cycle. During a write cycle, data are output on LAD0–LAD15 during the latter part of the cycle. LAD0 is the LSB, and LAD15 is the MSB. During the time the row address is output on LAD0–LAD14, status bit $\overline{\text{RF}}$ is output on LAD15. $\overline{\text{RF}}$ is active low at the start of a DRAM-refresh cycle (either $\overline{\text{RAS}}$-only or $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$). During the time that the column address is output on LAD0–LAD13, status bits $\overline{\text{TR}}$ and IAQ are output on LAD15 and LAD14, respectively. IAQ is active high during a read cycle in which the TMS34010 fetches an instruction word from the local memory. During all other cycles, IAQ is inactive low. $\overline{\text{TR}}$ is active low during shift-register-transfer cycles. (The level output on LAD14 during the high-to-low transition of $\overline{\text{CAS}}$ is always the same as the level output on $\overline{\text{TR}}/\overline{\text{QE}}$ during the high-to-low transition of $\overline{\text{RAS}}$.)

Note: The system designer must ensure that LRDY is not held low for so long that the TMS34010 is prevented from performing the necessary number of DRAM refresh cycles or is prevented from refreshing the display by performing a VRAM memory-to-shift-register cycle during horizontal retrace.

2.4 Video Timing Signals

The video timing signals (BLANK, HSYNC, and VSYNC) are used to control the horizontal and vertical sweep rates of the video monitor. They are also used to synchronize the display on the monitor to video data output from the VRAMs. Section 9 discusses video timing and screen refresh operations.

Table 2-4. Video Timing Signals

Signal	I/O	Description
HSYNC	I/O	*Horizontal Sync.* HSYNC is the horizontal sync signal used to control external video circuitry. It is programmed as either an input or an output by means of two control bits in the DPYCTL register. When configured as an output, the active-low horizontal sync signal is generated by the TMS34010's on-chip video timers. When configured as an input, the TMS34010 synchronizes its video timers to externally-generated horizontal sync pulses. Immediately following reset, HSYNC is configured as an input.
VSYNC	I/O	*Vertical Sync.* VSYNC is the vertical sync signal used to control external video circuitry. It is programmed as either an input or an output by means of a control bit in the DPYCTL register. When configured as an output, the active-low vertical sync signal is generated by the TMS34010's on-chip video timers. When configured as an input, the TMS34010 synchronizes its video timers to externally-generated vertical sync pulses. Immediately following reset, VSYNC is configured as an input.
BLANK	O	*Blanking.* BLANK is a composite blanking signal used to turn off the electron beam of a CRT during both horizontal and vertical retrace intervals. This signal may also be used to control the starting and stopping of the VRAM shift registers.
VCLK	I	*Video Clock.* VCLK is derived from the dot clock of the external video system and is used internally to drive the TMS34010's video timing logic. The signals output at the BLANK, HSYNC, and VSYNC pins are synchronous to VCLK. VCLK is not required to have any timing relationship with respect to INCLK; that is, VCLK and INCLK can be asynchronous. In order to read HCOUNT and VCOUNT registers reliably, VCLK should be held high during the read. In systems which do not use the video timing registers or require automatic screen refreshing, VCLK can be strapped high.

Note: During factory testing, the HSYNC and VSYNC pins are configured to scan data in and out of the two internal shift register scan paths.

2.5 Hold and Emulator Interface Signals

The TMS34010 hold interface permits other devices to request and be granted control of the local interface bus.

The emulator interface is used to control the TMS34010 when it is used for emulation. The RUN/EMU pin may remain unconnected in nonemulation applications.

Table 2-5. Hold and Emulator Interface Signals

Signal	I/O	Description
HOLD	I	*Hold Request.* The HOLD pin is driven active low by an external device to signal a request that the TMS34010 release ownership of the local memory bus. Once the TMS34010 has acknowledged the hold request via a hold acknowledge signal, the external device assumes ownership of the bus. The device must continue to assert its hold request until it has released the bus.
HLDA/EMUA	O	*Hold Acknowledge and Emulate Acknowledge.* The HLDA/EMUA pin is multiplexed between two functions – acknowledgment of hold requests and acknowledgment of emulation requests. The hold acknowledge signal (HLDA) is output during phases Q3 and Q4 of the local clock cycle. The emulate acknowledge signal (EMUA) is output during phases Q1 and Q2. HLDA is driven active low in response to a hold request from an external device, but not until the TMS34010 has released the bus to the requesting device. The device must delay taking possession of the bus until it has received an active HLDA signal. Once an active-low hold acknowledge signal has been transmitted during Q3–Q4, it will continue to be transmitted during Q3–Q4 of each local clock period until the external device ceases to assert its hold request. EMUA is driven active low to indicate to external circuitry that the TMS34010 has halted in response to an EMU command input on the RUN/EMU pin. HLDA/EMUA is also driven low when an EMU opcode is executed by the TMS34010, but only during phases Q1 and Q2 of a single LCLK1 cycle. Execution of an EMU opcode causes an active-low signal to be output at the HLDA/EMUA pin during phases Q1 and Q2, so external devices that generate hold requests should avoid interpreting these signals as hold acknowledgment.
RUN/EMU	I	*Run/Emulate.* This pin is defined as a no-connect during normal system operation. The RUN/EMU pin should *not* be pulled low except during factor testing or chip emulation. An internal pull-up load permits RUN/EMU to remain unconnected during normal use.

2.6 Power, Ground, and Reset Signals

Six TMS34010 pins are dedicated to ground and power supply. Section 8 provides more details about $\overline{\text{RESET}}$.

Table 2-6. Power, Ground, and Reset Signals

Signal	I/O	Description
V_{CC}	I	V_{CC} (2 pins). Two +5-volt power supply inputs.
V_{SS}	I	V_{SS} (4 pins). Four electrical ground inputs.
$\overline{\text{RESET}}$	I	*Reset.* $\overline{\text{RESET}}$ is pulled low to reset the device during normal operation. While $\overline{\text{RESET}}$ is asserted low, the internal registers of the TMS34010 are set to an initial known state, and all output and bidirectional pins are driven either to inactive levels or to high impedance. The behavior of the TMS34010 chip following reset depends on the level of the $\overline{\text{HCS}}$ input just prior to the low-to-high transition of $\overline{\text{RESET}}$. If $\overline{\text{HCS}}$ is low, the GSP begins executing the instructions pointer to by the reset vector. If $\overline{\text{HCS}}$ is high, the GSP is halted until a host processor writes a 0 to the HLT bit in the HSTCTL register. Transitions on the $\overline{\text{RESET}}$ pin are assumed to be asynchronous with respect to local clocks LCLK1 and LCLK2; the signal input on this pin is synchronized internally before it is used internally. During factory testing or chip emulation, $\overline{\text{RESET}}$ is used in conjunction with RUN/$\overline{\text{EMU}}$, $\overline{\text{HOLD}}$, $\overline{\text{LINT1}}$, and $\overline{\text{LINT2}}$ to configure the TMS34010 into the required test or emulation mode. As long as RUN/$\overline{\text{EMU}}$ is not pulled low, however, the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, $\overline{\text{LINT1}}$, and $\overline{\text{LINT2}}$ pins are configured for normal system operation.